What is claimed is:

1. A video output controller comprising:

a first storage device configured to store a DMA command list containing DMA commands;

a second storage device configured to secure frame buffers;

a video output buffer;

a DMA controller; and

a display controller comprising:

a DMA command list processor configured to determine which of the DMA commands contained in the DMA command list must be issued;

an initialize signal port configured to receive an initialize signal for starting initialization;

a step signal port configured to receive a step signal for starting the issuance of the DMA command; and

an external signal processor configured to provide the DMA command list processor with a timing signal for issuing a DMA command according to the initialize signal and step signal.

2. The video output controller of claim 1, wherein:

the DMA command list processor is initialized when the initialize signal port receives the initialize signal;

the display controller transfers the DMA command to the DMA controller when the step signal port receives the step signal; and

the DMA controller transfers, in response to the DMA command, data stored in the frame buffers of the second storage device to the video output buffer.

3. The video output controller of claim 1, wherein the DMA command list processor comprises:

a list header configured to hold a start position of the DMA command list; and

a list pointer configured to hold the position of a DMA command to be issued next.

4. The video output controller of claim 3, wherein:

when the initialize signal port receives the initialize signal, the DMA command list processor copies the start position held in the list header to the list pointer; and

when the step signal pointer receives the step signal, the DMA command list processor issues the DMA command indicated with the list pointer and updates the

list pointer according to predetermined rules.

5. The video output controller of claim 3, wherein:

the DMA command list comprises DMA command data and a pointer for next DMA command data to be issued in response to the step signal; and

the list pointer is updated by rewriting the list pointer with the pointer for next DMA command data.

6. The video output controller of claim 4, wherein:

elements contained in the DMA command list have an identical size and are aligned in order of activation; and

the list pointer is updated by adding the element size to the list pointer.

7. The video output controller of claim 1, wherein:

the external signal processor includes a counter configured to count the number of times of reception of the step signal, and when the counted number reaches a preset number of steps to complete the drawing of an image, the external signal processor sends an initialize timing signal to the DMA command list processor.

8. The video output controller of claim 7, wherein:

the DMA command list comprises DMA command

data and a pointer for next DMA command data to be issued in response to the step signal; and

the list pointer is updated by rewriting the list pointer with the pointer for next DMA command data.

9. The video output controller of claim 7, wherein:

elements contained in the DMA command list have an identical size and are aligned in order of activation; and

the list pointer is updated by adding the element size to the list pointer.

10. The video output controller of claim 4, wherein:

the DMA command list has a hierarchical structure with a plurality of levels;

the list pointer indicates a node at a first level; and

a plurality of DMA commands following a node that is lower than the node at the first level are activated at the time of DMA command issuance.

11. The video output controller of claim 10, wherein:

order of activation of DMA commands at a second level and at levels lower than the second level is predetermined;

the DMA command list includes a block flag to

control the activation of a hardware unit;

the display controller has a port to receive a third signal generated by the hardware unit; and

the display controller stops a DMA command for which the block flag is enabled until the third signal is received and releases the stopped DMA command upon detection of the third signal.

12. A video output controller comprising:

a video output buffer;

a DMA controller; and

a display controller comprising:

a DMA command list processor configured to determine which of the DMA commands contained in the DMA command list must be issued;

an initialize signal port configured to receive an initialize signal for starting initialization;

a step signal port configured to receive a step signal for starting the issuance of the DMA command; and

an external signal processor configured to provide the DMA command list processor with a timing signal for issuing a DMA command according to the initialize signal and step

signal.

13. The video output controller of claim 12, wherein:

the DMA command list processor is initialized when the initialize signal port receives the initialize signal;

the display controller transfers the DMA command to the DMA controller when the step signal port receives the step signal; and

the DMA controller transfers, in response to the DMA command, data stored in the frame buffers of the second storage device to the video output buffer.

14. The video output controller of claim 12, wherein the DMA command list processor comprises:

a list header configured to hold a start position of the DMA command list; and

a list pointer configured to hold the position of a DMA command to be issued next.

15. The video output controller of claim 14, wherein:

when the initialize signal port receives the initialize signal, the DMA command list processor copies the start position held in the list header to the list pointer; and

when the step signal pointer receives the step

signal, the DMA command list processor issues the DMA command indicated with the list pointer and updates the list pointer according to predetermined rules.

16. The video output controller of claim 14, wherein:

the DMA command list comprises DMA command data and a pointer for next DMA command data to be issued in response to the step signal; and

the list pointer is updated by rewriting the list pointer with the pointer for next DMA command data.

17. The video output controller of claim 15, wherein:

elements contained in the DMA command list have an identical size and are aligned in order of activation; and

the list pointer is updated by adding the element size to the list pointer.

18. The video output controller of claim 12, wherein:

the external signal processor includes a counter configured to count the number of times of reception of the step signal, and when the counted number reaches a preset number of steps to complete the drawing of an image, the external signal processor sends an initialize timing signal to the DMA command list processor.

19. A video card comprising:

a plurality of image processors configured to draw an image and generate image data to be stored in frame buffers;

a first storage device configured to store a DMA command list containing DMA commands;

a second storage device configured to secure the frame buffers;

a video output buffer;

a DMA controller; and

a display controller comprising:

a DMA command list processor configured to determine which of the DMA commands contained in the DMA command list must be issued;

an initialize signal port configured to receive an initialize signal for starting initialization;

a step signal port configured to receive a step signal for starting the issuance of the DMA command; and

an external signal processor configured to provide the DMA command list processor with a timing signal for issuing a DMA command according to the initialize signal and step signal.

20. The video card of claim 19, wherein:

the DMA command list processor is initialized when the initialize signal port receives the initialize signal;

the display controller transfers the DMA command to the DMA controller when the step signal port receives the step signal; and

the DMA controller transfers, in response to the DMA command, data stored in the frame buffers of the second storage device to the video output buffer.